Customer No.: 31561
Docket No.: 11690-US-PA
Application No.: 10/707,082

AMENDMENTS

In the Claims

1. (currently amended) A device for breaking a leakage current path existing in a defect memory cell in a memory array within a memory device, comprising:

a column selection line coupled to a first circuit block and adapted to select a column of a memory cell within a memory array, wherein the first circuit block ~~is capable of outputting~~ outputs a column turn-off signal when the defect memory cell is detected ;

a row selection line coupled to a second circuit block and adapted to select a row of the memory cell within the memory array, wherein the second circuit block ~~is capable of outputting~~ outputs a row turn-off signal when the defect memory cell is detected ;

a sensing amplifier; and

a switch device coupled to the memory cell, a power supply terminal, the sensing amplifier, the column selection line and the row selection line, wherein ~~only~~ when the memory cell is the defect memory cell, both the column selection line receives the column turn-off signal and the row selection line receives the row turn-off signal, so that the switch device is turned off ~~so as to~~ and ~~disconnect~~ a coupling between the power supply terminal and the defect memory cell is disconnected, thereby breaking the leakage current path existing in the defect memory cell.

2. (original) The device for breaking the leakage current path of claim 1, wherein the switch device further comprises:

a first switch coupled to the memory cell, the power supply terminal and the column selection line, wherein when the column selection line receives the column turn-

off signal, the first switch is turned off so that the power is not coupled to the memory cell, and when the column selection line does not receive the column turn-off signal, the power is coupled to the memory cell; and

a second switch coupled to the memory cell, the power supply terminal and the row selection line, wherein when the row selection line receives the row turn-off signal, the second switch is turned off so that the power is not coupled to the memory cell, and when the row selection line does not receive the row turn-off signal, the power is coupled to the memory cell.

3. (original) The device for breaking the leakage current path of claim 2, wherein each of the first switch and the second switch comprises a PMOS transistor or PMOSFET transistor.

4. (original) The device for breaking the leakage current path of claim 1, wherein the column turn-off signal and the row turn-off signal are controlled by a stand-by signal.

5. (currently amended) A method for breaking a leakage current path existing in a defect memory cell for a circuit having a memory array, the method comprising:

selecting a column selection line in response to a memory cell within a memory array;

selecting a row selection line in response to the memory cell within the memory array; ~~and~~

coupling a switch device to the memory cell, a power supply terminal, a sensing amplifier, the column selection line and the row selection line; and

turning off the switch device through coupling a column turn-off signal to the column selection line and a row turn-off signal to the row selection line when the memory cell is detected to be the defective memory cell and so that a power provided from a the power supply terminal is not coupled to the defect memory cell.

6. (previously amended) The method for breaking the leakage current path of claim 5, wherein the column turn-off signal and the row turn-off signal are controlled by stand-by signal.

7. (currently amended) A memory device, comprising:

a column selection line coupled to a first circuit block and adapted to select a column of a memory cell within a memory array, wherein the first circuit block is capable of outputting outputs a row column turn-off signal when a defect memory cell is detected;

a row selection line coupled to a second circuit block and adapted to select a row of the memory cell within the memory array, wherein the second circuit block is capable of outputting outputs a row turn-off signal when the defect memory cell is detected;

a sensing amplifier; and

a device for breaking a leakage current path, comprising a switch device coupled to the memory cell, a power supply terminal, the sensing amplifier, the column selection line and the row selection line, wherein only when the memory cell is the defect memory cell, both the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal, so that the switch device is turned off so as to disconnect and a coupling between the power supply terminal and the defect memory cell

is disconnected, thereby breaking a leakage current path existing in the defect memory cell.

8. (original) The memory device of claim 7, wherein the switch device further comprises:

a first switch coupled to the memory cell, the power supply terminal and the column selection line, wherein when the column selection line receives the column turn-off signal, the first switch is turned off so that the power is not coupled to the memory cell, and when the column selection line does not receive the column turn-off signal, the power is coupled to the memory cell; and

a second switch coupled to the memory cell, the power supply terminal and the row selection line, wherein when the row selection line receives the row turn-off signal, the second switch is turned off so that the power is not coupled to the memory cell, and when the row selection line does not receive the row turn-off signal, the power is coupled to the memory cell.

9. (original) The memory device of claim 8, wherein each of the first switch and the second switch comprises a PMOS transistor or PMOSFET transistor.

10. (original) The memory device of claim 7, wherein the column turn-off signal and the row turn-off signal are controlled by a stand-by signal.

11. (original) The memory device of claim 7, wherein the memory array comprises a DRAM array.

12. (previously amended) The memory device of claim 7, wherein the first circuit block is disposed between an original selection signal and the column selection line for

controlling the original selection signal and generating a final column selection signal from a stand-by signal and a fuse signal of the final column selection signal.

13. (currently amended) The memory device of claim 7, wherein the second circuit block ~~is capable of generating~~ generates a final row selection signal from a stand-by signal and a fuse signal of the final row selection signal.

14. (currently amended) The memory device of claim 12, wherein a state of the fuse signal of the final column selection signal and a state of the fuse signal of the final row selection signal for a selected normal memory cell are substantially lower than those of a selected defective memory cell and the column turn-off signal and the row turn-off signal are generated in response to the state of the fuse signal of the final column signal and state of the fuse signal of the row selection signal.